Team 16

Autonomous Neuromorphic Car

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PURDUE POLYTECHNIC

Customer Background

Dr. Robert Nawrocki

- Primary research in neuromorphic systems and flexible organic electronics
- Project will be used as a base for future research using organic components

Problem Statement / Scope of Work

- Implementation
  - Spiking Neural Network (SNN)
  - FPGA (Verilog & VHDL code)
  - Analog Grayscale Sensors
- Advantages of SNN Usage
  - Readily available hardware
  - Low power
  - Adaptable

Requirements

Req. #	DESIGN REQUIREMENTS	DESIGN TARGETS	VALIDATION
	RATIONALE		
1	Neural Network must be Hardware Implemented with low power requirements.	Runs off of USB power source (5V 0.5A [15])	Implement on FPGA powered by USB [12]
	This system must be portable as it will be used to control a small vehicle with limited battery power. The current control method of the vehicle uses an FPGA and to keep the design simple, the initial SNN will be implemented on a similar device [12].		
2	Neural Network must have an output react to input changes similar to biological reactions.	Outputs spike with consecutive changes in inputs.	System maneuvers through curves on testing tracks.
	The more biological-like process found in a Spiking Neural Network allows the system to be more adaptable and require less power [9].		
3	Initial AHDL based system follows track completely.	Vehicle completes track in both directions.	Run autonomous vehicle on track.
	Training system should be able to correctly run the full course [14].		

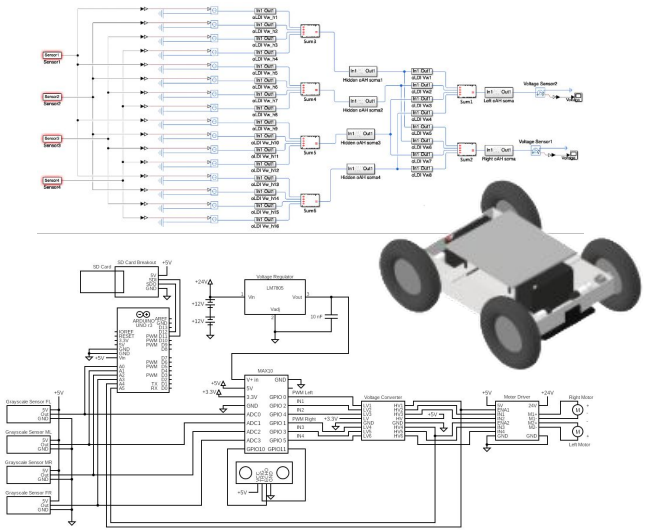
Experimentation and Concepts

SNN Output Frequencies at all input cases (W for whitte B for black)

	W W W B	W W B B	W W B W	W B B W	W B W W	B B W W	B W W W	
1 - initial system	1.00 k	7.315	16.129	28.571	12.484	244.1	1.44 k	Right
	1.44 k	204.3	12.484	28.249	15.82	7.013	1.00 k	Left
2 - Threshold Measurement	1.00 k	7.315	16.129	28.571	12.484	244.1	1.44 k	Right
	1.44 k	203.9	12.484	28.249	15.823	7.0126	1.00 k	Left
3 - Hidden Neurons	1.00 k	7.315	16.133	28.58	14.305	244	1.42 k	Right
	1.42 k	204.3	12.485	28.26	19.458	7.013	1.00 k	Left
4 - Forward and Brake cases	2.001 k	203.9	12.485	28.249	15.823	7.0126	1.00 k	Right
	1.999 k	7.315	16.129	28.571	12.485	244.1	1.427 k	Left
5 - Simplification	2.001 k	1.1113 k	12.483	28.24	15.823	7.0126	1.00 k	Right
	1.999 k	833.3	16.129	28.57	12.483	244.1	1.429 k	Left

A threshold was given when determining white and black lines on the track

Final Design



FMEA

PLANNING AND PREPARATION (STEP 1)					
Company Name	Purdue University				Subject
Engineering Loca	West Lafayette, IN				DFMEA Start Date
Customer Name	Robert Nawrocki				DFMEA Revision Date
Model Year(s)/P	2022				Cross Functional Tea
STRUCTURE ANALYSIS (STEP 2)			FUNCTION ANALYSIS (STEP 3)		
1. Next Higher Level	2. Focus Element	3. Next Lower Level or Characteristic Type	1. Next Higher Level Function and Requirement	2. Focus Element Function and Requirement	3. Next Lower Level Function and Requirement or Characteristic
Power Supply	12V battery	Battery Mounts	Supply power to the components of the car	Powers the motors to drive the car	battery mounts allow for maneuverability
Motor Control	H-Bridge Motor Driver Board	Motor controller plate	Take inputs from the DE10 to control the motors	Control the H-bridge motors	Electronic Mount
Board Control	DE-10 Lite Board	FPGA Board GPIO Ports	Provide Control signals based on input for sensors	Senses the track in order to orient the car correctly	sensors mounted under car to read the track

Testing

Track Testing			
Turn Type	Test	Details	Outcome
Straight	Place down 2 straight continuous tape paths for the car to follow	Start the vehicle on a stand to begin the test, plug the SD card in to the breakout module then set the car down onto the track. Let the car follow the track until it has completed the desired path of track then lift off the track and remove the SD card.	The outcome should produce the same frequency for the left and right output
90 Deg	Place down 2 paths or tape in roughly 5-6 segments to create a curve		Depending on the direction of the curve, the left or the right frequency should be slightly larger than the other causing the vehicle to turn

[9] B. Rajendran, A. Sebastian, M. Schmuker, N. Srinivasa, and E. Eleftheriou, "Low-Power Neuromorphic Hardware for Signal Processing Applications: A Review of Architectural and System-Level Design Approaches," IEEE Signal Processing Magazine, vol. 36, no. 6, pp. 97–110, Nov. 2019, doi: 10.1109/MSP.2019.2933719.

[12] T. Technologies, "Terasic - All FPGA Boards - MAX 10 - DE10-Lite Board." https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=218&No=1021&PartNo=2#heading (accessed Sep. 12, 2022).

[14] M. Vanmali, M. Last, and A. Kandel, "Using a neural network in the software testing process," Int. J. Intell. Syst., vol. 17, pp. 45–62, Jan. 2002, doi: 10.1002/int.1002.

[15] "What are the Maximum Power Output and Data Transfer Rates for the USB Standards?" https://resources.pcb.cadence.com/blog/2020-what-are-the-maximum-power-output-and-data-transfer-rates-for-the-usb-standards (accessed Sep. 12, 2022).